A MULTI CHANNEL CHOPPER MODULATED NEURAL RECORDING SYSTEM

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Abstract - **Presented herein is a fully integrated low-noise CMOS multi-channel amplifier for neural recording applications. The circuit employs the chopper modulation technique to reduce the effect of flicker noise and DC offset. A reduced area design implementation is achieved by trading off the increased noise margin performance of the chopper modulator for minimal amplifier area and analog multiplexing of the recording sites. A fully differential topology is used for the signal path to improve noise immunity. The analog amplifier exhibits 56 dB of gain with a 115 kHz bandwidth and a common mode rejection ratio (CMRR) of 80 dB. Simulation results show a total input referred noise less than 16 nV/√Hz. The system power consumption is approximately 750 μWatts. The fully integrated system was designed in ABN 1.6-um single poly n-well CMOS process.**

Keywords - **Neural recording, chopper technique, switching noise, flicker noise**

I. INTRODUCTION

The steady advance in CMOS IC processing technologies has stimulated the rapid growth of electrode array micro-sensors used for neural recording applications. The use of a single silicon substrate for both CMOS integrated circuits and neuron cultures provides an attractive approach to experimentally monitor and stimulate the electrical activity of neural arrays. The ability to record neural signals using CMOS circuitry has previously been demonstrated [1]. Some of the work involves "in vivo" recording of the neural signals [1], in which the recording sites are inserted to the live animals whereas others study "in vitro" recording of the neural signals, in which the neurons are cultured outside of the body [2].

In [1], a neural recording probe with multiple recording sites and CMOS signal processing circuitry was fabricated on a shared silicon substrate. The front-end system consisted of 32 recording sites with 8 channels allocated for analog signal pre-amplification followed by an 8-to-1 analog multiplexer. The pre-amplifiers were designed with large area PMOS input devices to partially address the 1/f noise while high pass filtering was used to minimize signal DC drift. In [2], an "in-vitro" characterization of 2-D network of neurons was implemented. However, the analog amplifiers were not integrated with the recording sites. Harb et. al. [3] describes an implantable instrumentation amplifier for low-amplitude signal amplification using the chopper stabilization technique. However, the signal amplification is implemented with two amplifier stages that include a selective filter, resulting in increased silicon area. Furthermore, the system is applicable only for single channel recording.

In this paper we present a fully integrated amplifier circuit used in neural recording systems. The system is designed to stimulate and monitor the electrical activity of a large population of neurons using an array of recording sites within a shared substrate. The recording sites are implemented with "open-gate, metal –free" insulated-gate field-effect transistors for direct coupling of the neuron and silicon without the interfering metal interface exhibited in microelectrode arrays [4]. Each recording site is multiplexed into larger cells (typically 4 to 8 recording sites) to minimize area.

The compact amplifier cells use the well-known chopper technique [4], [5] instead of large amplifier input devices and high pass filters to reduce problems associated with flicker noise and DC offset. A local voltage reference is used to eliminate DC drift of the recorded signals via differential path amplification. Compact analog switches are use to multiplex the recording signal before amplification to minimize area and power. This paper discusses the front-end architecture and circuit implementation of the multi-channel amplifier.

II. ARCHITECTURE

The top-level architecture of the neural recording system is shown in Fig. 1. The front-end system consists of an analog multiplexer, a chopper modulator, a cascode amplifier, a chopper demodulator and a low-pass filter. The inputs to the system are 4-to-1 multiplexed using an analog multiplexer. These signals are referenced to an unbiased location in the system, which is labeled as REF in the figure, to minimize the effects of the DC drift of the neural signals. The selected signal is modulated via a fully differential chopper modulator, which up-converts the signal to the chopper frequency. The signal is then amplified and demodulated back to the baseband by the output chopper modulator. The final low-pass filter stage removes the remaining out-of-band noise for subsequent analog-to-digital conversion and signal processing.

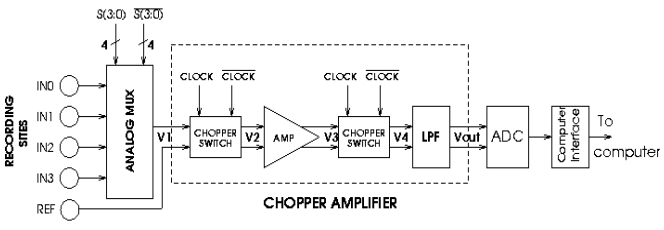

Fig. 1. Toplevel architecture

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Abstract

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The 4-channel analog multiplexer is shown in Fig. 2. The input and select signals are labeled IN0-IN3 and S0-S3, respectively. Charge injection cancellation is achieved by inserting "dummy" switches, which are driven by complementary select signals [5]. The "dummy" switches are also inserted between the recording sites and main switches to isolate the effect of charge feed-through from the neural signal.

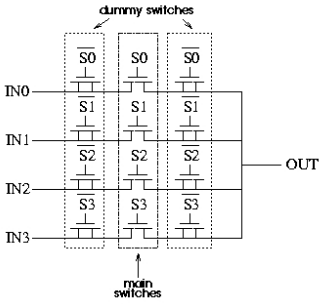

Fig. 2. 4-channel analog multiplexer

A major concern of very low frequency signal amplification is the inherent 1/f device noise of MOS transistors. Furthermore, provided good transistor matching, a realistic CMOS amplifier may exhibit approximately +/- 20mV of input referred DC offset [6]. This constant DC offset will severely degrade the dynamic range of the high gain amplifier used for neural signal amplification. The chopper modulator/demodulator circuit shown in Fig. 3 is used to mitigate these effects [5]. This circuit is used to modulate the signal to the odd harmonics of the chopping frequency. The chopping frequency of the system can be chosen according to (1).

$$f_{corner} + BW_{signal} < f_{chop} < BW_{amp} - BW_{signal} \qquad (1)$$

Where f_{corner} is the noise corner frequency, BW_{signal} is the input signal's bandwidth, f_{chop} is the chopper frequency and BW_{amp} is the main amplifier's bandwidth. In our system, the noise corner is calculated to be 10 KHz.

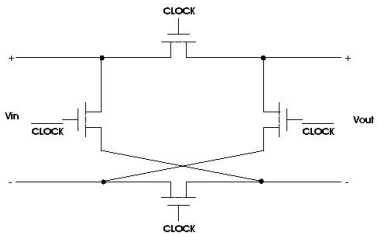

Fig. 3. Chopper modulator/demodulator

The chopper modulator, however, injects a residual offset to the signal due to nonidealities of the MOS switches, such as clock feedthrough and charge injection. This residual offset is minimized due to the differential signal path and the small time constant of the residual offset, as explained next. (1) Since the chopper modulator has a differential path, the residual offset will appear as a common-mode voltage at the output; therefore the common mode noise voltages will cancel each other. This requires a proper matching of the switches [5]. (2) This residual offset has a very small time constant compared to clock period of the chopper. For example, a typical 10k Ohm switch on resistance and 1 pF capacitance at the amplifier's input will result in a 10-ns time constant, which is very small compared to possible chopper periods. Therefore most of the energy is located at much higher frequencies than the chopper frequency. Most of this energy will be low-pass filtered by the main amplifier, since it has a finite bandwidth [5].

After modulation the signal passes through an amplifier stage. The fully differential amplifier and common-mode feedback circuitry are shown in Fig. 4. A cascode amplifier topology is used because it achieves the highest gain with a single stage. The area of the input transistors can be reduced because their flicker noise contribution will be filtered by the chopper technique. This amplifier exhibits a gain of 56 dB with a 115 kHz bandwidth. This configuration results in more than 80 dB CMRR.

To improve the tuning range during testing, several chopping frequencies will be used for comparison. Furthermore, connecting an external capacitor to the output stage of the amplifier can reduce the bandwidth of the main amplifier for added flexibility. Making the amplifier's bandwidth twice the chopper frequency will result in minimum residual offset that passes through the amplifier [5].

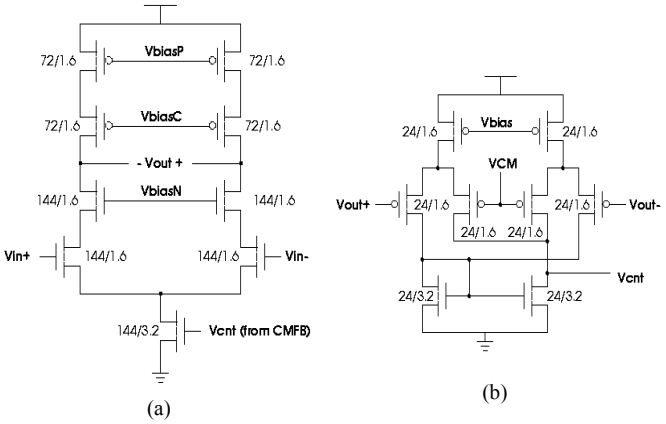

Fig. 4: (a) Cascode amplifier (b) Common mode feedback circuit

The low-pass filter is implemented with a second order gm-c filter. A block diagram of a 2nd order biquad filter is shown in Fig. 5. The transfer function of this filter is given in (2).

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{G_{m1}G_{m2}}{C_1C_2}}{s^2 + s\frac{G_{m3}}{C_2} + \frac{G_{m2}G_{m4}}{C_1C_2}} \qquad (2)$$

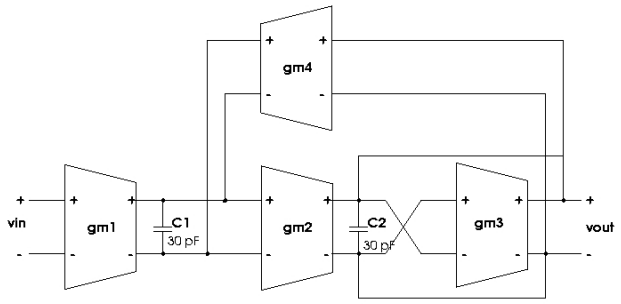

Fig. 5. Low pass filter

For the gm stages, linearized transconductance circuits have been used [9]. [10], which is shown in Fig. 6. The transconductance of this circuit is given in (7). It depends on bias current I_d and sizes of the transistors M_1 and M_3'. Eq. (8) defines k_3 and k_1. In this circuit, M_1 and M_3' operates in triode region, which improves the linearity of the circuit. Linearity is rather important in our system, because the input to the low-pass filter has a large signal swing. The common-mode voltages of the transconductance circuits are set by the common-mode feedback circuit shown in Fig. 4b.

$$G_m = \frac{4k_3\sqrt{k_1 I_d}}{4k_3 + k_1} \tag{3}$$

$$k_k = \frac{\mu_k C_{ox}}{2}\frac{W_k}{L_k} \tag{4}$$

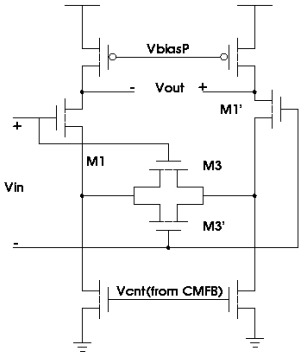

Fig. 6. Linearized transconductance

In this application, the 3-dB cut-off frequency of the filter is chosen to be 5 kHz because most neural signals has less than 5 kHz bandwidth, and DC gain is chosen as 1.1, because the inputs to the low-pass filter are already amplified. The gm and capacitance values that satisfy these specifications are listed in Table 1.

Table 1: Characteristics of the low-pass filter

Gm1	753 nS
Gm2	1.179 uS
Gm3	787 nS
Gm4	674 nS
C1=C2	30 pF

III. RESULTS AND DISCUSSION

A transient simulation of one channel of the system is shown in Fig. 7. The curves at left represent the voltages shown in Fig. 1 and the curves at right represent the Discrete Fourier Transform (DFT) of the transients. The input signal has 500uV amplitude and 1 kHz frequency. In order to simulate flicker noise, a sinusoidal voltage source, which has 200uV amplitude and 500 Hz frequency, is inserted between chopper modulator and the amplifier. This is, in fact, an overestimation of the flicker noise. The chopping frequency has been set to 20 kHz. The output signal shows that most of the noise has been low-pass filtered. In reality, flicker noise at 500 Hz would be much smaller, in the order of microvolts, which can be derived from (1).

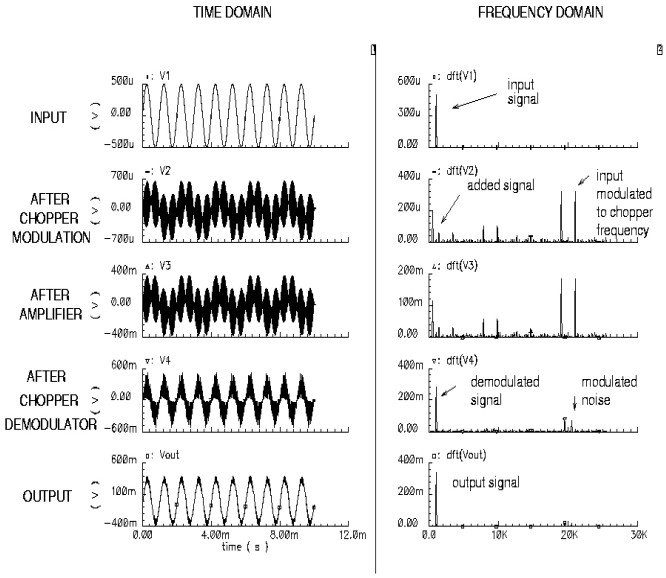

Fig. 7. Simulation results

The summary of the simulation results is given Table 2.

Table 2: Summary of the results

Supply Voltage	5V
Power Consumption	<750 uW
DC Gain	650
Amplifier Bandwidth	115 kHz
CMRR	<80 dB
Input referred noise	<16 nV/rt(Hz)

This paper describes the architecture for a multichannel neural recording amplifier, and uses the chopper modulation technique. This system was designed using ABN 1.6 micron process. After chip fabrication, the system will be integrated with a neural recording environment. The recording sites will be created using "open-gate, metal –free" insulated-gate field-effect transistors, which is proposed in [4]. The neurons

will be placed on the metal-free gate oxide of a field-effect transistor. The source will be biased with a positive voltage to bring the FET into strong inversion. The neurons are then to be stimulated to measure the current waveforms.

Further work will include the integration of the A/D converter and interface with a DSP unit to provide a system level solution for neural recordings. This will include a recording chamber, a measurement setup and computer analysis.

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